Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**G = GATE**

**S = SOURCE**



**G**

**Top Material: Al**

**Backside Material: Ti/Ni/V/Ag**

**Bond Pad Size: G = .0125” X .0176”**

**Backside Potential: Drain**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .070” X .095” DATE: 4/25/22**

**MFG: FAIRCHILD THICKNESS .008” P/N: FDD86102**

**DG 10.1.2**

#### Rev B, 7/19/02